REMARKS

Favorable consideration and allowance of the claims of the present application are respectfully requested.

In the present Official Action, Claim 1 stands rejected as allegedly being anticipated by Lee et al. (US Patent Pub. 2005/0186750) (hereinafter "Lee").

Claims 2-13 were additionally rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Lee et al. in view of Zhu et al. (US Patent Pub. 2005/0189589) (hereinafter "Zhu").

With respect to the rejection of Claim 1, applicants respectfully disagree.

Claim 1 is directed to a MOS (metal oxide semiconductor) transistor device having gate stress engineering with SiGe and/or Si:C. Respectfully, Lee is directed to a Heterojunction Bipolar Transistors (HBT) and is particularly directed to the formation of an intrinsic base region (element 6, Fig. 5 of Lee) for such an HBT device using a novel method for forming a SiGe base.

As Lee is directed to a method for fabricating an extrinsic base region for a HBT it is non-analogous and can not be anticipatory of the present invention which is directed to a method for forming a novel MOS transistor device including a stacked gate structure. That is, a MOSFET device to which the present invention is directed, is different from HBT in structure and function. For examples, MOSFET devices have to have an insulator gate dielectric or gate oxide between gate and body; however, no insulator is necessary for a HBT to work. That is, the Lee does not teach a gate dielectric layer over the substrate. The only

dielectric layers taught in Lee are STI structures (elements 12, Fig. 5 of Lee) and insulator layer 16 that defines an HBT base region process window where a base contact layer 18 is to be formed. Moreover, layer 16, while stated as a thickness of 300 Å – 800 Å (see ¶[0019] of Lee) is much thicker than a gate oxide dielectric layer typically is (e.g., less than 100 Å).

Moreover, Lee's method requires the formation of a seed layer 20B over the STI region of "reduced" grain size (see ¶[0020], pages 2-3 of Lee). To the contrary, in the present invention, it is intended that the α-Si or poly –Si layer 14 deposited over the gate oxide dielectric layer is a first stressed film layer of "large" grain size, as set forth in Claim 1. Thus, Lee would teaches away the formation of a large grain size layer stress film layer formed over a dielectric layer.

Furthermore, the HBT device in Lee will not introduce stress in the (substrate) layer 14 due to the SiGe layer 22. However, stresses in semiconductor substrate layer (channel region 10 underlying the gate oxide 12 in Fig. 1 of the present application) produced by the structure claimed in Claim 1 of the present application is key and constitutes a main feature for performance enhancement of MOSFETs. That is, channel stress can be introduced by patterning the gate stack as is claimed in Claim 1, e.g., etching Si/SiGe/Si stacked layer to apply stress to the channel of the MOSFET device. To this end, Lee does not even mention, much less claim, the formation of any stresses in their structure, only to improving electrical conductivity between the base and the base contact region (see ¶[0021], page 3 of Lee). Therefore, we can not learn any stress information from Lee.

Thus, respectfully, as the HBT device of Lee is quite different from the present invention as claimed in amended Claim 1, the Examiner is respectfully requested to withdraw the rejection of independent Claim 1 under 35 U.S.C. 102(b).

With respect to the rejection of Claims 2-13 as being unpatentable over Lee in view of Zhu, applicants respectfully disagree.

Zhu et al, in all, the embodiment described, teaches how to build a MOSFET device by applying a stressed film under the channel or body of a MOSFET. However, the present invention as claimed in Claims 1 and dependent claims, teaches how to apply stress to the channel from the gate, i.e., <u>above the channel</u>. Thus, the structure claimed in the present invention (Claim 1, et seq.) is quite different from that in Zhu. For example, there is no disclosure of any stressed materials in the gate described in Zhu. A stressed gate is the key consideration for improving nFET/pFET device performance in the present application. Similarly, there is no stressed film under the MOS device channel claimed in the present invention, while Zhu explicitly teaches the formation of stressed films under the channel which is the key component of Zhu.

As such, it can not be said that the teachings are combinable or would render the present inventions claimed in Claims 2-13 obvious as the combination does not teach or suggest stressed channels by gate stress engineering as in the present invention.

Thus, respectfully, the Examiner is respectfully requested to withdraw the rejection of Claims 2-13 under 35 U.S.C. 103(a).

In view of the foregoing, this application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a

telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

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